



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,546	10/23/2003	John R. Chase	ALTRP098/A1185	3624
51501 7590 08/02/2010 WEAVER AUSTIN VILLENEUVE & SAMPSON LLP - ALTERA ATTN: ALTERA P.O. BOX 70250 OAKLAND, CA 94612-0250				
EXAMINER LO, SUZANNE				
ART UNIT 2128		PAPER NUMBER		
NOTIFICATION DATE 08/02/2010		DELIVERY MODE ELECTRONIC		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTO@wavsip.com

# Office Action Summary

**Application No.**

10/693,546

**Applicant(s)**

CHASE, JOHN R.

**Examiner**

SUZANNE LO

**Art Unit**

2128

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 June 2010.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-32 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-32 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 23 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO/GS/US)  
4) ☐ Interview Summary (PTO-413)  
5) ☐ Notice of Informal Patent Application  
6) ☐ Other: \_\_\_\_\_  
Paper No(s)/Mail Date \_\_\_\_\_

**DETAILED ACTION**

1. Claims 1-32 have been presented for examination.

**Claim Rejections - 35 USC § 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
  2. Ascertaining the differences between the prior art and the claims at issue.
  3. Resolving the level of ordinary skill in the pertinent art.
  4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
2. **Claims 1-2, 5, 17-21, 25-28, and 30** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Whitten (U.S. Patent No. 5,805,795)** in view of **Bening et al. ("Optimizing Multiple EDA Tools within the ASIC Design Flow")** in further view of **Dustin ("Automated Testing Tools")**.

As per claim 1, Whitten is directed to a method comprising: generating a plurality of test designs (column 8, lines 15-21), the plurality of test designs having varied characteristics to allow testing of a design automation tool (column 4, lines 45-55), wherein generating one of the plurality of test designs comprises: selecting a plurality of submodules from a design module library (column 4, line 64- column 5, line 2 and column 5, lines 22-52), wherein a

probabilistic function is applied to select the plurality of submodules of different types from the library (**column 6, line 63 – column 7, line 9**); applying the plurality of test designs to test the design automation tool (**column 8, lines 15-21**) but fails to explicitly disclose instantiating an input/output (I/O) structure of a top level module, the top level module having input and output pins; parameterizing the plurality of submodules from the design module library for interconnection with the top level module, the plurality of submodules having input and output lines; providing logic to interconnect the plurality of parameterized submodules as well as to connect the plurality of parameterized submodules to various input and output pins of the top level module, and wherein the said selecting the plurality of submodules is constrained based on a hardware family of the one of the test designs, wherein the hardware family is selected from a plurality of hardware families.

Bening teaches creating a test design for an EDA tool comprising instantiating the I/O structure of a top level module, the top level module having input and output pins (**page 47, 1<sup>st</sup> column, Design methodologies, 2<sup>nd</sup> paragraph**); selecting a plurality of submodules from a design module library (**page 51, column 2, 2<sup>nd</sup> paragraph**); parameterizing the plurality of submodules from the design module library for interconnection with the top level module, the plurality of submodules having input and output lines (**page 54, 1<sup>st</sup> column, 4<sup>th</sup> paragraph**); providing logic to interconnect the plurality of parameterized submodules as well as to connect the plurality of parameterized submodules to various input and output pins of the top level module (**pages 52-53, scan chain hookup**) and wherein the said selecting the plurality of submodules is constrained based on a hardware family of the one of the test designs, wherein the hardware family is selected from a plurality of hardware families (**page 51, “Optimizing physical design”, instantiating vendor-specific macro cells**). It would have been obvious to an ordinary person skilled in the art to combine the method of generating a plurality of test

designs of Whitten with the creation of test designs with EDA tools of Bening in order to optimize EDA tools **(Bening, page 46, 1<sup>st</sup> paragraph)**.

The combination of Whitten and Bening fails to explicitly disclose *determining whether a predetermined number of the test designs for testing the design automation tool has been generated*. Dustin teaches determining whether a predetermined number of the test designs for testing a system or application has been generated **(page 4, 1<sup>st</sup> paragraph)**. Whitten, Bening, and Dustin are analogous art because they are all directed to generating test designs. It would have been obvious to an ordinary person skilled in the art at the time of the invention to combine the method of generating a plurality of test designs of Whitten and Bening with the determination step of Dustin in order to gain insight into the effectiveness of the test suite **(Dustin, page 4, 1<sup>st</sup> paragraph)**.

**As per claim 2**, the combination of Whitten, Bening and Dustin already discloses the method of claim 1, wherein the design automation tool is used to implement hardware descriptor language designs on a programmable chip **(Bening, page 46, 1<sup>st</sup> column, 2<sup>nd</sup> paragraph)**.

**As per claim 5**, the combination of Whitten, Bening and Dustin already discloses the method of claim 1, wherein the design automation tool is a synthesis or a place and route tool **(Bening, page 52, scan chain hookup)**.

**As per claim 28**, the combination of Whitten, Bening and Dustin already discloses the method of claim 1, further comprising selecting a plurality of submodules upon said determining that the predetermined number of the test designs is not generated **(page 4, 1<sup>st</sup> paragraph, help produce the integration test)**.

**As per claims 17-21, and 30**, Whitten discloses a computer system **(column 4, lines 22-33)**, comprising: memory operable to hold information associated with a design module library, a processor coupled to memory, the processor configured to execute a method with the

same limitations of claim 1 and wherein a submodules of different types are randomly selected from the library (**column 6, lines 63-67**) is therefore rejected over the same art combination.

**As per claim 25-27**, Whitten is directed to an apparatus for generating test a testbench (**column 4, lines 22-33**), the apparatus comprising: means for a method with the limitations of claim 1 and is therefore rejected over the same art combination.

**3. Claims 4, 6-13, 15, and 22-24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Whitten (U.S. Patent No. 5,805,795) in view of Bening et al. ("Optimizing Multiple EDA Tools within the ASIC Design Flow") in further view of Dustin ("Automated Testing Tools") **in further view of Zaidi et al. (U.S. Patent Application Publication 2002/0038401 A1)**.

**As per claim 4**, the combination of Whitten, Bening and Dustin already discloses the method of claim 1, but fails to explicitly disclose wherein instantiation constraints are used to select the plurality of submodules. Zaidi teaches wherein instantiation constraints are used to select the plurality of submodules (**[0085]**). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of generating a plurality of IC test designs with a testbench of Whitten, Bening and Dustin with the instantiation constraints of Zaidi in order to provide pre-designed SoC architecture to decrease development time (**Zaidi, [0013], [0016]**).

**As per claim 6**, the combination of Whitten, Bening and Dustin already discloses the method of claim 1, but fails to explicitly to disclose wherein providing logic to interconnect the plurality of parameterized modules comprises identifying inputs and outputs. Zaidi teaches wherein providing logic to interconnect the plurality of parameterized modules comprises identifying inputs and outputs (**[0048]-[0060]**). It would have been obvious to one of ordinary

skill in the art at the time of the invention to combine the method of generating a plurality of IC test designs with a testbench of Whitten, Bening and Dustin with the interconnecting logic of Zaidi in order to provide pre-designed SoC architecture to decrease development time (Zaidi, [0013], [0016]).

**As per claim 7**, the combination of Whitten, Bening, Dustin and Zaidi already discloses the method of claim 6, wherein inputs comprise input pins of the top level module, submodule output lines, and registers (Zaidi, [0048]-[0060]).

**As per claim 8**, the combination of Whitten, Bening, Dustin and Zaidi already discloses the method of claim 6, wherein outputs comprise output pins of the top level module, submodule input lines, and registers (Zaidi, [0048]-[0060]).

**As per claim 9**, the combination of Whitten, Bening, Dustin and Zaidi already discloses the method of claim 8, wherein providing logic to interconnect the plurality of parameterized modules classifying inputs and outputs as clock lines, control lines, and data lines (Bening, page 54, module code, signals q, clk, and d).

**As per claim 10**, the combination of Whitten, Bening, Dustin and Zaidi already discloses the method of claim 8, wherein generating one of the plurality of test designs further comprises: generating randomized logic (Zaidi, [0048]-[0060])

**As per claim 11**, the combination of Whitten, Bening, Dustin and Zaidi already discloses the method of claim 10, randomized is generated logic to drive outputs (Zaidi, [0047]).

**As per claim 12**, the combination of Whitten, Bening and Zaidi already discloses the method of claim 10, wherein generating randomized logic comprises directly wiring outputs to inputs, generating a logic expression using inputs, generating a mathematical expression using inputs, or generating decision logic (Zaidi, [0047]).

**As per claim 13**, the combination of Whitten, Bening, Dustin and Zaidi already discloses the method of claim 6, wherein parameterizing the plurality of submodules comprises defining interfaces, data width, and the type of signal for input and output lines associated with the submodule (**Bening, page 54, module code, output [1:0] q**).

**As per claim 15**, the combination of Whitten, Bening, Dustin and Zaidi already discloses the method of claim 6, wherein generating one of the plurality of test design further comprises selecting a clock structure for each output (**Zaidi, [0047]**).

**As per claims 22-24**, Whitten discloses a computer system (**column 4, lines 22-33**), comprising: memory operable to hold information associated with a design module library, a processor coupled to memory, the processor configured to execute a method with the same limitations of claim 6-8 and is therefore rejected over the same art combination.

4. **Claims 14 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Whitten (U.S. Patent No. 5,805,795) in view of Bening et al. ("Optimizing Multiple EDA Tools within the ASIC Design Flow") in further view of Dustin ("Automated Testing Tools") in further view of Zaidi et al. (U.S. Patent Application Publication 2002/0038401 A1) **in further view of Goossens ("Design of Heterogeneous ICs for Mobile and Personal Communication Systems")**.

**As per claim 14**, the combination of Whitten, Bening, Dustin and Zaidi is directed to the method of claim 6, wherein submodules comprise memory and timers (**[0037]**) but fails to disclose wherein submodules comprise adders and phase lock loops. Goossens teaches submodules comprising of adders and phase lock loops (**page 524-525, Figure 1, Section 3.2**). Whitten, Bening, Dustin, Zaidi, and Goossens are analogous art because they are all from the same field of endeavor, validating an IC. It would have been obvious to one of ordinary skill in



the art at the time of the invention to combine the method of generating a plurality of IC test designs with a testbench of Whitten, Bening, Dustin and Zaidi with the adders and phase lock loops of Goossens in order to allow the design of heterogeneous IC architecture (**page 524, Section 1**).

**As per claim 16**, the combination of Whitten, Bening, Dustin, and Zaidi is directed to the method of claim 15, but fails to specifically disclose wherein clock structures include a plurality of synchronous and asynchronous structures. Goossens teaches clock structures that include a plurality of synchronous and asynchronous structures (**page 525-526, Section 3.3**). Whitten, Bening, Zaidi and Goossens are analogous art because they are all from the same field of endeavor, validating an IC. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of generating a plurality of IC test designs with a testbench of Whitten, Bening, Dustin and Zaidi with the clock structures of Goossens in order to implement handshaking, protocol control, and synchronization functionalities for heterogeneous IC architecture (**page 525-526, Section 3.3**).

5. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Whitten (U.S. Patent No. 5,805,795) in view of Bening et al. ("Optimizing Multiple EDA Tools within the ASIC Design Flow") in further view of Dustin ("Automated Testing Tools") **in further view of Rajsuman (U.S. Patent No. 6,678,645)**.

**As per claim 3**, the combination of Whitten, Bening and Dustin already discloses the method of claim 1, but fails to explicitly disclose wherein the plurality of submodules comprises a memory module and a Digital Signal Processor (DSP) Core. Rajsuman teaches generating a plurality of test designs of an ASIC including DSP and memory submodules (**column 1, lines 16-29**). Whitten, Bening, and Rajsuman are analogous art because they are all from the same

field of endeavor, validating an IC. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of generating a plurality of test designs of Whitten, Bening, and Dustin with the submodules of Rajsuman in order to verify the entire system the way it would be used by the end user (**Rajsuman, column 3, lines 34-38**).

6. **Claims 29, 31-32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Whitten (U.S. Patent No. 5,805,795) in view of Bening et al. ("Optimizing Multiple EDA Tools within the ASIC Design Flow") in further view of Dustin ("Automated Testing Tools") **in further view of Barford (U.S. Patent Application Publication 2003/0139906 A1)**.

**As per claim 29**, the combination of Whitten, Bening and Dustin already discloses the method of claim 1, but fails to explicitly disclose wherein the predetermined number is provided by a user. Barford teaches wherein the predetermined number of test designs in a test suite is provided by a user ([0075]-[0076]). Whitten, Bening, Dustin and Barford are analogous art as they are all from the same field of endeavor, generating test designs. It would have been obvious to an ordinary person skilled in the art at the time of the invention to combine the method of generating test designs of Whitten, Bening, and Dustin with the user designated test design number of Barford in order to provide user control in an automated testing system.

**Claim 31** is directed to the computer system comprising a processor configured to execute a method with the same limitations as claim 29 and is therefore rejected over the same prior art combination.

**Claim 32** is directed to an apparatus comprising means for a method with the limitations of claim 29 and is therefore rejected over the same prior art combination.

**Response to Arguments**

7. Applicant's arguments filed 06/14/10 have been fully considered but they are not persuasive.
8. Applicant's arguments regarding the amended limitations and new claims have been considered but are moot in view of the new grounds of rejection.

In response to Applicant's argument that Whitten and Bening either alone or in combination do not related to testing a design automation tool, in accordance to Applicant's own admission on page 11 that Whitten relates to methods, computer program products, computer systems, and apparatuses for testing software products, the Applicant is asked to explain how a design automation tool is not a software product. A cursory internet search with the keywords "Altera", "eda" and "tools" immediately identifies the webpage "EDA Tool Support Resource Center" at the address: <http://www.altera.com/support/software/eda-tool-support/sof-eda-tool-support.html> wherein EDA tool Support is a subcategory of "Design **Software**" (emphasis added). As electronic design automation tools are known and commonly identified as software products, Whitten relates to testing a design automation tool as Whitten relates to testing any software product.

In view of the above, the Examiner has not found any subject matter in the claims or specification that can overcome the combination of prior art teachings.

**Conclusion**

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. The prior art made of record is not relied upon because it is cumulative to the applied rejection. These references include:

1. U.S. Patent No. 6,477,691 B1 issued to Bergamashi/Rab et al. on 11/05/02.
  2. U.S. Patent Application Publication No. 2004/0015792 A1 published by Kubista on 01/22/04.
  3. U.S. Patent No. 6,053,947 issued to Parson on 04/25/00.
  4. "ASIC to FPGA Design Methodology & Guidelines" published by Altera in July 2003.
  5. U.S. Patent No. 7,085,702 issued to Hwang et al. on 08/01/06.
  6. U.S. Patent Application Publication No. 2004/0210798 A1.
  7. U.S. Patent No. 6,907,550 B2 issued to Webser et al. on 06/14/05.
  8. U.S. Patent No. 6,378,088 B1 issued to Mongan on 04/23/02.
  9. U.S. Patent No. 6,189,116 B1 issued to Mongan et al. on 02/13/01.
  10. U.S. Patent No. 6,334,207 issued to Joly et al. on 12/25/01.
  11. U.S. Patent No. 5,754,760 issued to Warfield on 05/19/98.
10. All Claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suzanne Lo whose telephone number is (571)272-5876. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2297. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/SL/  
07/27/10

/Hugh Jones/

Primary Examiner, Art Unit 2128